

NAME

ntb_hw_amd - AMD Non-Transparent Bridge driver

SYNOPSIS

To compile this driver into your kernel, place the following lines in your kernel configuration file:

```
device ntb  
device ntb_hw_amd
```

Or, to load the driver as a module at boot, place the following line in loader.conf(5):

```
ntb_hw_amd_load="YES"
```

The following sysctls are supported in this driver

dev.ntb_hw.X.info

Reading this sysctl will give the basic details like the number of memory windows, scratchpads and doorbells exposed by the NTB on the local host to access the devices beyond the bridge. It also provides details about the masked doorbells, translation address and size limit of each exposed memory window and link status information.

DESCRIPTION

The **ntb_hw_amd** driver provides support for the Non-Transparent Bridge (NTB) hardware in AMD EPYC processor family. The Non-Transparent Bridge does not look as a regular PCI bridge, but as PCI endpoint device, hiding the devices behind it. The driver hides details of hardware on the other side, but exposes memory windows, scratchpads and doorbells to access the other side via hardware independent KPI to ntb(4) subsystem.

The hardware provides 2 (both 64-bit) or 3 (one 32-bit and two 64-bit) memory windows to the other system's memory, up to 16 scratchpad registers and 16 doorbells to communicate with and interrupt the other system respectively.

CONFIGURATION

The NTB configuration should be set by BIOS. This includes enabling NTB, choosing topology (only NTB-to-Root Port mode is supported now), role of the host in the topology. This needs to be done on both systems.

The BAR size for memory windows is configured to 1 MiB by default.

SEE ALSO

if_ntb(4), ntb(4), ntb_transport(4)

AUTHORS

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